REMARKS

It is important to remember the problem the present invention is addressing. The following quote from the Background of the Invention is helpful in remembering the significant problem that has arisen regarding the tradeoff between performance and system cost.

"Most computer consumers are urging the industry to provide an increase in the rate of data communication (e.g., Internet, WANs, LANs, token ring, etc.) over conventional communication media (e.g., copper wire, cable, wireless, etc.). Yet, the personal computer (PC) market and the PC consumer will generally not accept an increase in performance at the expense of a severe increase in system cost. Therefore, it is advantageous for the cost of newly designed data communication systems (e.g., ADSL modems, cable modems, wireless systems, V.90 modems and the like) to remain flat or even decrease over time while simultaneously accommodating improved performance.

Historically, the modem integrated circuit (IC) industry has responded to the desire for enhanced performance by designing and manufacturing much more complex digital signal processors (DSPs) that can provide more MIPS (millions of instructions per second) or use by modem algorithms. While these faster and more complex DSP ICs may significantly enhance performance, many of these new DSP products are too expensive or too power-intensive to use within the sub-$1000 PC market or within the growing number of low-cost, low-power, embedded or hand-held modem systems. In short, the market will not accept incrementally adding up to several hundred dollars in modem DSP hardware to a PC or hand-held device where such addition increases the overall cost of these devices by 20% or more. Furthermore, many older, low-cost, existing DSPs simply do not have the MIPS capability to perform all the requisite data pump functions needed in modern DMT modem systems. Therefore, it has been very difficult to offer the consumer increased data communication rates at reduced costs when using conventional modem architectures that execute all modem operations on a DSP engine.

Some systems have opted to entirely eliminate the DSP from the modem solution to reduce cost. These systems, referred to as "soft modems", are simply a collection of software functions or algorithms that are placed into the general purpose global memory of a PC and executed entirely on the host processor of the PC (e.g., PowerPC™ 604 or Pentium™ II). Many

of these "soft modem" solutions are being provided to the market at a price that is cheaper than the base manufacturing costs of many modem DSPs. However, the soft modem solution consumes a significant portion of the MIPS of the host processor, whereby the host processor is generally too busy processing incoming data to quickly perform real-time tasks for the current computer user. Therefore, while the soft modem is a significant advance and very useful in some applications, it is not a viable solution for every consumer in all situations.

Therefore, a need exists in the industry for a system that provides adequate high-end performance (e.g., enough performance to more efficiently implement higher rate communication protocols like asymmetric digital subscriber line (ADSL), cable modem, and G.lite implementations), at a cost that is attractive to consumers, in a flexible manner, without consuming user-noticeable amounts of host CPU processing power."

Applicants respectfully note that claim 13 expressly requires a single digital signal processor that performs "frequency domain equalization (FEQ) operations, time domain equalization (TEQ) operations, fast fourier transform (FFT) operations, inverse fast fourier transform (iFFT) operations, and encoding/decoding operations on a serial stream of data provided through the analog interface". Modlin does not teach or even suggest this. Modlin teaches a much more expensive approach having a separate prior art transmitter (see FIG. 1A) and a separate prior art receiver (see FIG. 1B), neither of which perform all of the functions expressly required by claim 13. Also, In FIG. 3, Modlin teaches a receiver only, which also performs forward error correction (see Modlin, col. 10, lines 10-54), but which does not perform all of the functions required by the express language of claim 13. Again it is very important to remember that the goal achieved by the present invention was an increase in performance with little or no increase in system cost. Modlin teaches separate circuitry for the transmitter and separate circuitry for the receiver. Thus, Modlin teaches away from the present invention. Also, since Modlin teaches double the circuitry, the circuitry taught in Modlin is presumably at least double the cost over the present invention.

The Examiner has stated that "the error correction taught by Modlin takes place in the FEC unit 164, which is analogous to the functionality of the second processor in the present invention" (Office Action dated 8/2/04, page 3, last line to page 4 second line). Claim 13 states that the second processor is coupled to the data bus for receiving packets of data from the digital signal processor. Applicants are confused as to which block(s) in FIG. 3 of Modlin the Examiner

believes performs the required functions performed by the digital signal processor (namely "performs "frequency domain equalization (FEQ) operations, time domain equalization (TEQ) operations, fast fourier transform (FFT) operations, inverse fast fourier transform (iFFT) operations, and encoding/decoding operations on a serial stream of data provided through the analog interface"). FIG. 3 of Modlin teaches only a first insertion unit 308 and a CRC unit 306 that provide data to FEC unit 310. And neither the first insertion unit 308 nor the CRC unit 306 perfoms the required functions performed by the claimed digital signal processor (namely "performs "frequency domain equalization (FEQ) operations, time domain equalization (TEQ) operations, fast fourier transform (FFT) operations, inverse fast fourier transform (iFFT) operations, and encoding/decoding operations on a serial stream of data provided through the analog interface").

Thus, Modlin does not teach, and in fact teaches away from, the functionality and structure of claim 13. Also, Applicants agree with the Examiner that "Modlin does not explicitly teach at least one operation performed by the first processor and the second processor to be dynamically reassigned" (Office Action dated 8/2/04, page 4, lines 3-4).

Applicants refer now to Carmon (US Patent No. 5,404,522). The Examiner has quoted from the title and abstract of Carmon but has no where shown that Carmon teaches "wherein at least one operation performed by one of the digital signal processor and the host CPU can be dynamically reassigned to a different one of the digitial signal processor and the host CPU". Applicants have found no such teaching in Carmon. In fact, Carmon teaches away from the claimed approach by teaching "if sufficient resources are not available, the DSP task request placed by the user will be rejected and an appropriate user error message will be given" (Carmon, col. 9, lines 15-18). And again, "If sufficient resource exists as shown in FIG. 6, the tasks will be loaded and the functions will begin operation in the DSP. Otherwise, an appropriate error message will be generated by the user's host PC to notify the use that the requested tasks will not be loaded" (Carmon, col. 11, lines 56-61). Carmon does not teach dynamically reassigning an operation. In fact, Carmon teaches away from such an approach. Instead, Carmon teaches providing an error message if the DSP cannot carry out a requested operation.

Applicants respectfully assert that Claim 20 and all dependent claims are allowable for at least the reasons given above for claim 13.

Applicants believe the present application is in condition for allowance which action is respectfully solicited. Please contact me if there are any issues regarding this communication or the current Application.

Applicants respectfully request a telephone interview with the Examiner if there are any remaining issues which prevent this patent application from being allowed.

Respectfully submitted,

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